What is Claimed is:

1. A method of detecting phase of transitions in a data signal relative to a reference clock signal comprising:

producing a plurality of phase-shifted versions of the reference clock signal;

using each of the versions in order of magnitude of phase shift to sample the data signal;

comparing the samples to a training pattern that is initially aligned with training data in the data signal;

re-aligning the training pattern with the training data each time use of one of the versions causes the training pattern to become misaligned with the training data; and

analyzing information including which of the versions caused misalignment to approximate the phase of the transitions.

2. The method defined in claim 1 further comprising:

selecting one of the versions for use in sampling the data signal after the training data based at least in part on the phase of the transitions as approximated in the analyzing.

3. The method defined in claim 1 wherein each of the phase-shifted versions is delayed by the same amount of delay relative to an immediately less phase-shifted one of the versions.

4. The method defined in claim 3 wherein the delay is selected so that the unit interval is not an integer multiple of the delay.

5. The method defined in claim 4 wherein the plurality includes n of the versions, and wherein n times the delay is greater than two unit intervals.

6. The method defined in claim 2 wherein the data signal has a unit interval corresponding to duration of each bit in the data signal, and wherein the selecting selects one of the versions that is near the center of the unit interval.

7. Apparatus for detecting phase of transitions in a data signal relative to a reference clock signal comprising:

a plurality of delay circuit elements for producing a plurality of phase-shifted versions of the reference clock signal;

selection circuitry for selectively selecting each of the versions in order of magnitude of phase shift as a sampling clock signal for sampling the data signal;

comparison circuitry for comparing samples of the data signal, taken using the sampling clock signal, to a training pattern;

alignment circuitry for initially aligning the training pattern with training data in the data signal and for subsequently re-aligning the training pattern with the training data each time use of one of the versions causes the training pattern to become misaligned with the training data; and

circuitry for monitoring which of the versions caused misalignment of the training pattern with the training data.

8. The apparatus defined in claim 7 wherein the delay circuit elements are connected in series and all have the same amount of delay.

9. The apparatus defined in claim 8 wherein the amount of delay is selected so that the unit interval is not an integer multiple of the amount of delay.

10. The apparatus defined in claim 9 wherein the plurality includes n of the versions, and wherein n times the amount of delay is greater than two unit intervals.

11. The apparatus defined in claim 7 wherein the selection circuitry includes means for advancing to a next one of the versions after the comparison circuitry detects an instance of data corresponding to the training pattern in the data signal or a non-correspondence between the data signal and the training pattern.

12. The apparatus defined in claim 7 wherein the alignment circuitry comprises:

means for selectively recirculating the training pattern in synchronism with the sampling clock signal.

13. The apparatus defined in claim 12 wherein the means for selectively recirculating comprises:

means for halting the recirculating during initial aligning and subsequent re-aligning of the training pattern with the training data.

14. The apparatus defined in claim 7 wherein the circuitry for monitoring comprises:

means for determining the approximate phase of the data signal relative to the reference clock signal based at least in part on which of the versions cause the misalignment.

15. The apparatus defined in claim 7 further comprising:

means for selecting one of the versions for use in producing a retimed version of the data signal.

16. A programmable logic device including apparatus as defined in claim 7.

17. A digital processing system comprising:

processing circuitry;

a memory coupled to the processing circuitry; and

a programmable logic device as defined in claim 16 coupled to the processing circuitry and the memory.

18. A printed circuit board on which is mounted a programmable logic device as defined in claim 16.

19. The printed circuit board defined in claim 18 further comprising:

a memory mounted on the printed circuit board and coupled to the programmable logic device.

20. The printed circuit board defined in claim 18 further comprising:

processing circuitry mounted on the printed circuit board and coupled to the programmable logic device.

21. A method of determining an amount of phase shift of a reference clock signal that will render that signal advantageous for use in sampling a data signal that may be skewed relative to the reference clock signal comprising:

aligning a training pattern with training data in the data signal;

using a sampling clock signal based on the reference clock signal to sample the data signal and advance the training pattern;

comparing the advancing training pattern to the data signal samples until the training pattern is complete or until a lack of correspondence between the training pattern and a data signal sample is detected;

shifting the phase of the sampling clock signal by a predetermined amount after completion of the comparing;

re-aligning the training pattern with the training data if the comparing is completed by detection of a lack of correspondence;

repeating the using, comparing, shifting, and re-aligning until the total amount of phase shift due to the shifting is at least greater than the duration of any two successive bits in the data signal; and

sampling the data signal subsequent to the training data with a phase that is determined based at least in part on information as to which iterations

of the comparing were completed by detection of a lack of correspondence.